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EXAMINER	
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ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,246	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/31/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-33 are pending.

2. The office acknowledges the following papers:

Drawings filed on 2/2/2004,

Foreign priority papers filed on 3/15/2004.

Priority

3. This application claims priority to provisional application 60/400,391. The effective filing date for those claims which have proper support in the provisional application is 7/31/2002.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claims 2-4 recite the limitation "Java bytecode" must be shown or the feature(s) canceled from the claim(s). Instructions from both ISA's contain the Java bytecode must be shown in the figures to show the limitations from claims 2-4. Also, the method claims of 9 to 20 must be shown or the feature(s) canceled from the claim(s). Also, claims 21-33 contain limitations describing the switching on modes depending on different situations must be shown or the feature(s) canceled from the claim(s). A program showing the instruction flow and mode change based on temporary and permanent instructions would be sufficient to show the limitations of claims 21-33. The method claims must be entered

because the drawings contain no elements that show how the two modes are switched between one another. No new matter should be entered. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

Specification

5. The disclosure is objected to because of the following informalities:

6. The section titled cross-reference to related applications cites cases related, but leaves out the serial numbers. The serial numbers of the applications should be added, or the patent numbers should be added if applicable.

7. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware.

8. Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claim 2-4 and 7 are rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly

connected, to make and/or use the invention. The limitation "Java Impdep1 Bytecode" isn't contained in the specification to enable one of ordinary skill in the art without undue experimentation.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 1 is rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 6,832,305), in view of So (U.S. 6,944,746).

13. As per claim 1:

Park disclosed a CPU and coprocessor, comprising:

Decode logic adapted to decode instructions from a first instruction set in a first mode and adapted to decode instructions from a second instruction set in a second mode (Park: Figure 1 element 170 and 123, column 3 lines 25-37 and column 4 lines 1-30)(The decoder units are able to decode two instruction sets, with element 170 decoding in one mode and element 123 decoding in another mode. Thus having the same functionality.), wherein the decode logic is adapted to switch temporarily or permanently from one mode to another (Park: Figure 1 element 113, column 4 lines 1-30)(The predecode logic causes the mode of execution to change.);

Pre-decode logic coupled to the decode logic and adapted to operate in parallel

with the decode logic (Park: Figure 1 element 113, column 4 lines 1-30); and

Wherein the first and second instruction sets each comprises an instruction that temporarily switches the decode logic from one mode to another for at least one subsequent instruction (Park: Figure 1 element 110 and 120, column 3 lines 25-37 and column 4 lines 1-30)(The unsupported instructions on element 110 cause a temporary switch in the mode of execution. A followed supported instruction causes a temporary switch in the mode of execution back to the original mode. Thus having the same functionality.).

Park failed to teach decode logic adapted to decode instructions from a first instruction set in a first mode and adapted to decode instructions from a second instruction set in a second mode on a single processor.

However, So disclosed decode logic adapted to decode instructions from a first instruction set in a first mode and adapted to decode instructions from a second instruction set in a second mode on a single processor (So: Figure 5 element 522, column 8 lines 6-42).

An advantage of having a decode unit that decodes multiple ISA's on one processor is that it avoids duplication of logic and lowers costs of the processing system. Costs will be lowered from having one decoder running instead of two. Additional savings would be achieved through power savings from having to run one unit instead of two. One of ordinary skill in the art would have been motivated by decreased costs and power savings to implement a single decode unit on a single processor instead of a decode unit on multiple processors. Thus, it would have been

obvious to one of ordinary skill in the art at the time of the invention to implement a single decoder unit on one processor to decode multiple ISA's for the advantage of decreased costs and power savings.

14. Claims 2-4 and 7 are rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 6,832,305), in view of So (U.S. 6,944,746), further in view of Seal et al. (U.S. 6,965,984).

15. As per claim 2:

Park and So disclosed the processor of claim 1.

Park and So failed to teach wherein the first and second instruction sets each comprises a Java Impdep1 Bytecode that temporarily switches the 'decode logic from one mode to another.

However, Seal disclosed wherein the first and second instruction sets each comprises a Java Impdep1 Bytecode that temporarily switches the decode logic from one mode to another (Seal: Figure 20, column 17 lines 38-67 continued to column 18 lines 1-9).

There are many well-known data processing systems capable of processing multiple ISA's (Seal: Column 1 lines 13-16). It would have been obvious to one of ordinary skill in the art that an ISA executing java bytecodes could be combined with an ISA such as x86 or PowerPC. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add an ISA executing java bytecodes to the current combination of Park and So.

16. As per claim 3:

Park and So disclosed the processor of claim 1.

Park and So failed to teach wherein the first instruction set comprises a first reserved Java Bytecode that temporarily switches the decode logic from the first mode to the second mode for at least one subsequent instruction, wherein the at least one subsequent instruction belongs to the second instruction set.

However, Seal disclosed wherein the first instruction set comprises a first reserved Java Bytecode that temporarily switches the decode logic from the first mode to the second mode for at least one subsequent instruction, wherein the at least one subsequent instruction belongs to the second instruction set (Seal: Figure 20, column 17 lines 38-67 continued to column 18 lines 1-9).

There are many well-known data processing systems capable of processing multiple ISA's (Seal: Column 1 lines 13-16). It would have been obvious to one of ordinary skill in the art that an ISA executing java bytecodes could be combined with an ISA such as x86 or PowerPC. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add an ISA executing java bytecodes to the current combination of Park and So.

17. As per claim 4:

Park and So disclosed the processor of claim 1.

Park and So failed to teach wherein the second instruction set comprises a second reserved Java Bytecode that temporarily switches the decode logic from the second mode to the first mode for at least one subsequent instruction, wherein the at

least one subsequent instruction belongs to the first instruction set.

However, Seal disclosed wherein the second instruction set comprises a second reserved Java Bytecode that temporarily switches the decode logic from the second mode to the first mode for at least one subsequent instruction, wherein the at least one subsequent instruction belongs to the first instruction set (Seal: Figure 20, column 17 lines 38-67 continued to column 18 lines 1-9).

There are many well-known data processing systems capable of processing multiple ISA's (Seal: Column 1 lines 13-16). It would have been obvious to one of ordinary skill in the art that an ISA executing java bytecodes could be combined with an ISA such as x86 or PowerPC. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add an ISA executing java bytecodes to the current combination of Park and So.

18. As per claim 7:

Park, So, and Seal disclosed the processor of claim 6, wherein thy instruction that permanently switches the decode logic from the first mode to the second mode succeeds a Java Impdep1 Bytecode (Seal: Figure 20, column 17 lines 38-67 continued to column 18 lines 1-9).

19. Claims 5-6 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 6,832,305), in view of So (U.S. 6,944,746), further in view of Gorishek, IV et al. (U.S. 6,308,255).

20. As per claim 5:

Park and So disclosed the processor of claim 1.

Park and So failed to teach wherein the first instruction set comprises an instruction that permanently switches the decode logic from the first mode to the second mode.

However, Gorishek disclosed wherein the second instruction set comprises an instruction that permanently switches the decode logic from the first mode to the second mode (Gorishek: Figure 8 element 140, column 15 lines 46-67 continued to column 16 lines 1-3)(The Go instruction tells that there will be a large sequence of emulation processing to come and that the mode of execution will change so that the emulation program is executed until a stop instruction occurs. Thus having the same functionality.).

An advantage of having a Go and Stop instruction that permanently switches the mode of execution is that the other half of the processing system is known not to be active. In this case, the inactive half of the processing system could be put in a power save mode in order to save power in the processing system. One of ordinary skill in the art would have been motivated by the power savings to add permanent execution mode switch instructions to the processing system of Park and So. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add permanent switch instruction for the advantages of saving power for the inactive half of the processing system.

Park, So, and Gorishek failed to teach wherein the first instruction set comprises an instruction that permanently switches the decode logic from the first mode to the second mode.

However, it would have been obvious to one of ordinary skill in the art that if the second ISA has an instruction to switch modes from the first ISA to the second ISA, then the first ISA could also have a similar instruction. An advantage for the first ISA having such an instruction is that it could alert a program to execute for the second ISA that it has finished and the program for the second ISA can start executing. Thus, it would have been obvious to one of ordinary skill in the art that the first ISA could have a permanent switch instruction similar to the second ISA instruction for the advantage of alerting a program to execute for the second ISA that a program for the first ISA has completed.

21. As per claim 6:

Park and So disclosed the processor of claim 1.

Park and So failed to teach wherein the second instruction set comprises an instruction that permanently switches the decode logic from the first mode to the second mode.

However, Gorishek disclosed wherein the second instruction set comprises an instruction that permanently switches the decode logic from the first mode to the second mode (Gorishek: Figure 8 element 140, column 15 lines 46-67 continued to column 16 lines 1-3)(The Go instruction tells that there will be a large sequence of emulation processing to come and that the mode of execution will change so that the emulation

program is executed until a stop instruction occurs. Thus having the same functionality.).

An advantage of having a Go and Stop instruction that permanently switches the mode of execution is that the other half of the processing system is known not to be active. In this case, the inactive half of the processing system could be put in a power save mode in order to save power in the processing system. One of ordinary skill in the art would have been motivated by the power savings to add permanent execution mode switch instructions to the processing system of Park and So. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add permanent switch instruction for the advantages of saving power for the inactive half of the processing system.

22. As per claim 8:

Park and So disclosed the processor of claim 1

Park and So failed to teach wherein the second instruction set comprises an instruction that permanently switches the decode logic from the second mode to the first mode.

However, Gorishek disclosed wherein the second instruction set comprises an instruction that permanently switches the decode logic from the second mode to the first mode (Gorishek: Figure 8 element 140, column 15 lines 46-67 continued to column 16 lines 1-3)(The Stop instruction tells that the large sequence of emulation instructions has ended and that host processor instructions can continue to execute. Thus having the same functionality.).

An advantage of having a Go and Stop instruction that permanently switches the mode of execution is that the other half of the processing system is known not to be active. In this case, the inactive half of the processing system could be put in a power save mode in order to save power in the processing system. One of ordinary skill in the art would have been motivated by the power savings to add permanent execution mode switch instructions to the processing system of Park and So. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add permanent switch instruction for the advantages of saving power for the inactive half of the processing system.

23. Claims 9-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 6,832,305), in view of Gorishek, IV et al. (U.S. 6,308,255).

24. As per claim 9:

Park disclosed a method of decoding instructions from a first and second instruction sets, comprising:

Decoding instructions from the first instruction set in a first mode and decoding instructions from a second instruction set in the second mode (Park: Figure 1 element 170 and 123, column 3 lines 25-37 and column 4 lines 1-30)(The decoder units are able to decode two instruction sets, with element 170 decoding in one mode and element 123 decoding in another mode. Thus having the same functionality.);

Switching the decoding from one mode to another for one instruction (Park: Figure 1 element 170 and 123, column 3 lines 25-37)(The decoder units are able to

decode two instruction sets, with element 170 decoding in one mode and element 123 decoding in another mode. Thus having the same functionality.);

Park failed to teach switching the decoding permanently from one mode to another.

However, Gorishek disclosed switching the decoding permanently from one mode to another (Gorishek: Figure 8 element 140, column 15 lines 46-67 continued to column 16 lines 1-3)(The Go instruction tells that there will be a large sequence of emulation processing to come and that the mode of execution will change so that the emulation program is executed until a stop instruction occurs. Thus having the same functionality.).

An advantage of having a Go and Stop instruction that permanently switches the mode of execution is that the other half of the processing system is known not to be active. In this case, the inactive half of the processing system could be put in a power save mode in order to save power in the processing system. One of ordinary skill in the art would have been motivated by the power savings to add permanent execution mode switch instructions to the processing system of Park and So. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add permanent switch instruction for the advantages of saving power for the inactive half of the processing system.

25. As per claim 10:

Park and Gorishek disclosed the method of claim 9, wherein the step of switching the decoding from one mode to another for the one instruction comprises detecting a

temporary instruction that indicates the one instruction belongs to another instruction set (Park: Figure 113, column 4 lines 1-30)(The predecode logic detects an instruction belonging to another ISA and switches execution mode temporarily. Thus having the same functionality.).

26. As per claim 11:

Park and Gorishek disclosed the method of claim 10, wherein the step of switching the decoding from one mode to another comprises switching from the first mode and the second mode for the one instruction, wherein the one instruction belongs to the second instruction set (Park: Figure 113, column 4 lines 1-30; Column 3 lines 25-37)(The predecode logic detects an instruction belonging to another ISA and switches execution mode temporarily. Thus having the same functionality.).

27. As per claim 12:

Park and Gorishek disclosed the method of claim 10, wherein the step of switching the decoding from one mode to another comprises switching from the second mode and the first mode for the one instruction, wherein the one instruction belongs to the first instruction set (Park: Figure 113, column 4 lines 1-30; Column 3 lines 25-37)(The predecode logic detects an instruction belonging to another ISA and switches execution mode temporarily. Upon detecting an instruction that belongs the original ISA, the execution mode is switched back. Thus having the same functionality.).

28. As per claim 13:

Park and Gorishek disclosed the method of claim 10, wherein the first and second instruction sets each comprises the temporary instruction (Park: Column 4 lines

1-30)(Each instruction is predecoded to determine which mode of execution will occur. Thus having the same functionality.).

29. As per claim 14:

Park and Gorishek disclosed the method of claim 9, wherein the step of switching the decoding permanently from mode to another comprises detecting a temporary instruction that indicates the one instruction belongs to another instruction set (Park: Figure 113, column 4 lines 1-30; Column 3 lines 25-37)(Gorishek: Figure 8 element 140, column 15 lines 46-67 continued to column 16 lines 1-3)(The predecoder would detect the Go instruction to show the execution mode has changed temporarily. Thus having the same functionality.).

30. As per claim 15-17:

Claims 15-17 essentially recite the same limitations of claim 6. Therefore, claims 15-17 are rejected for the same reasons as claim 6.

31. As per claim 18-20:

Claims 18-20 essentially recite the same limitations of claim 8. Therefore, claims 18-20 is rejected for the same reasons as claim 8.

32. Claims 21-26 are rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 6,832,305), in view of So (U.S. 6,944,746), in view of Gorishek, IV et al. (U.S. 6,308,255).

33. As per claim 21:

Park disclosed a CPU and coprocessor, comprising:

Decode logic adapted to decode instructions from a first instruction set in a first mode and adapted to decode instructions from a second instruction set in a second mode (Park: Figure 1 element 170 and 123, column 3 lines 25-37 and column 4 lines 1-30)(The decoder units are able to decode two instruction sets, with element 170 decoding in one mode and element 123 decoding in another mode. Thus having the same functionality.);

Pre-decode logic coupled to the decode logic and adapted to pre-decode instructions in parallel with the decode logic wherein the pre-decode logic pre-decodes for a temporary instruction that switches the decode logic from one mode to another for a subsequent instruction (Park: Figure 1 element 113, column 4 lines 1-30)(The predecode unit detects an unsupported instruction and switches modes of execution. Thus having the same functionality.); and

Wherein the first and second instruction sets each comprises the temporary instruction (Park: Figure 1 element 113, column 4 lines 1-30)(The predecode unit detects an unsupported instruction and switches modes of execution. The predecode unit then detects a supported instruction afterwards that switches back the mode of execution to its original state. Thus having the same functionality.);

Park failed to teach decode logic adapted to decode instructions from a first instruction set in a first mode and adapted to decode instructions from a second instruction set in a second mode on a single processor.

Wherein the second instruction set further comprises a first permanent instruction and a second permanent instruction.

However, So disclosed decode logic adapted to decode instructions from a first instruction set in a first mode and adapted to decode instructions from a second instruction set in a second mode on a single processor (So: Figure 5 element 522, column 8 lines 6-42).

An advantage of having a decode unit that decodes multiple ISA's on one processor is that it avoids duplication of logic and lowers costs of the processing system. Costs will be lowered from having one decoder running instead of two. Additional savings would be achieved through power savings from having to run one unit instead of two. One of ordinary skill in the art would have been motivated by decreased costs and power savings to implement a single decode unit on a single processor instead of a decode unit on multiple processors. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a single decoder unit on one processor to decode multiple ISA's for the advantage of decreased costs and power savings.

Park and So failed to teach wherein the second instruction set further comprises a first permanent instruction and a second permanent instruction.

However, Gorishek disclosed wherein the second instruction set further comprises a first permanent instruction and a second permanent instruction (Gorishek: Figure 8 element 140, column 15 lines 46-67 continued to column 16 lines 1-3)(The Go instruction tells that there will be a large sequence of emulation processing to come and that the mode of execution will change so that the emulation program is executed until a stop instruction occurs. The Stop instruction tells that the large sequence of emulation

instructions has ended and that host processor instructions can continue to execute. Thus having the same functionality.).

An advantage of having a Go and Stop instruction that permanently switches the mode of execution is that the other half of the processing system is known not to be active. In this case, the inactive half of the processing system could be put in a power save mode in order to save power in the processing system. One of ordinary skill in the art would have been motivated by the power savings to add permanent execution mode switch instructions to the processing system of Park and So. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add permanent switch instruction for the advantages of saving power for the inactive half of the processing system.

34. As per claim 22:

Park, So, and Gorishek disclosed the processor of claim 21, wherein the temporary instruction indicates that the subsequent instruction belongs to another instruction set and causes the decode logic to switch from one mode to another (Park: Figure 1 element 113, column 4 lines 1-30; Column 3 lines 25-37)(The predecoder detects the temporary instructions and switches modes of execution. Thus having the same functionality.).

35. As per claim 23:

Park, So, and Gorishek disclosed the processor of claim 22 wherein the decode logic temporarily switch from the first mode to the second mode, and wherein the subsequent instruction belongs to the second instruction set (Park: Figure 1 element

113, column 4 lines 1-30; Column 3 lines 25-37)(The predecoder detects an unsupported instruction and switches execution modes. Thus having the same functionality.).

36. As per claim 24:

Park, So, and Gorishek disclosed the processor of claim 22, wherein the decode logic temporarily switches from the second mode to the first mode, and wherein the subsequent instruction belongs to the first instruction set (Park: Figure 1 element 113, column 4 lines 1-30; Column 3 lines 25-37)(The predecoder detects an unsupported instruction and switches execution modes. At a later point, the predecoder detects a supported instruction and switches execution to the original mode. Thus having the same functionality.).

37. As per claim 25:

Park, So, and Gorishek disclosed the processor of claim 21, wherein the subsequent instruction is the first permanent instruction that switches the decode logic permanently from the first the mode to the second mode (Gorishek: Figure 8 element 140, column 15 lines 46-67 continued to column 16 lines 1-3)(The Go instruction tells that there will be a large sequence of emulation processing to come and that the mode of execution will change so that the emulation program is executed until a stop instruction occurs. Thus having the same functionality.).

38. As per claim 26:

Park, So, and Gorishek disclosed the processor of claim 21, wherein the second permanent instruction permanently switches the decode logic from the second mode to

the first mode (Gorishek: Figure 8 element 140, column 15 lines 46-67 continued to column 16 lines 1-3)(The Stop instruction tells that the large sequence of emulation instructions has ended and that host processor instructions can continue to execute. Thus having the same functionality.).

39. Claims 27-33 are rejected under 35 U.S.C. §103(a) as being unpatentable over Park et al. (U.S. 6,832,305), in view of So (U.S. 6,944,746), in view of Gorishek, IV et al. (U.S. 6,308,255).

40. As per claim 27:

Park disclosed a system, comprising:

Main processor (Park: Figure 1 element 110, column 3 lines 25-37); and

Co-processor coupled to the main processor (Park: Figure 1 element 120, column 3 lines 25-37), the main processor (It would have been obvious to one of ordinary skill in the art that the decode logic and predecode logic could have been moved from the co-processor to the main processor. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.) comprising:

Decode logic adapted to decode instructions from a first instruction set in a first mode and adapted to decode instructions from a second instruction set in a second mode (Park: Figure 1 element 170 and 123, column 3 lines 25-37 and column 4 lines 1-30)(The decoder units are able to decode two instruction sets, with element 170 decoding in one mode and element 123 decoding in another

mode. Thus having the same functionality.);

Pre-decode logic coupled to the decode logic and adapted to pre-decode instructions in parallel with the decode logic, wherein the pre-decode logic pre-decodes for a temporary instruction (Park: Figure 1 element 113, column 4 lines 1-30)(The predecode unit detects an unsupported instruction and switches modes of execution. Thus having the same functionality.); and

Wherein the first and second instruction set each comprises the temporary instruction (Park: Figure 1 element 113, column 4 lines 1-30)(The predecode unit detects an unsupported instruction and switches modes of execution. The predecode unit then detects a supported instruction afterwards that switches back the mode of execution to its original state. Thus having the same functionality.);

Park failed to teach decode logic adapted to decode instructions from a first instruction set in a first mode and adapted to decode instructions from a second instruction set in a second mode on a single processor.

Wherein the second instruction set further comprises a first permanent instruction and a second permanent instruction.

However, So disclosed decode logic adapted to decode instructions from a first instruction set in a first mode and adapted to decode instructions from a second instruction set in a second mode on a single processor (So: Figure 5 element 522, column 8 lines 6-42).

An advantage of having a decode unit that decodes multiple ISA's on one

processor is that it avoids duplication of logic and lowers costs of the processing system. Costs will be lowered from having one decoder running instead of two. Additional savings would be achieved through power savings from having to run one unit instead of two. One of ordinary skill in the art would have been motivated by decreased costs and power savings to implement a single decode unit on a single processor instead of a decode unit on multiple processors. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a single decoder unit on one processor to decode multiple ISA's for the advantage of decreased costs and power savings.

Park and So failed to teach wherein the second instruction set further comprises a first permanent instruction and a second permanent instruction.

However, Gorishek disclosed wherein the second instruction set further comprises a first permanent instruction and a second permanent instruction (Gorishek: Figure 8 element 140, column 15 lines 46-67 continued to column 16 lines 1-3)(The Go instruction tells that there will be a large sequence of emulation processing to come and that the mode of execution will change so that the emulation program is executed until a stop instruction occurs. The Stop instruction tells that the large sequence of emulation instructions has ended and that host processor instructions can continue to execute. Thus having the same functionality.).

An advantage of having a Go and Stop instruction that permanently switches the mode of execution is that the other half of the processing system is known not to be active. In this case, the inactive half of the processing system could be put in a power

save mode in order to save power in the processing system. One of ordinary skill in the art would have been motivated by the power savings to add permanent execution mode switch instructions to the processing system of Park and So. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add permanent switch instruction for the advantages of saving power for the inactive half of the processing system.

41. As per claim 28:

Claim 28 essentially recites the same limitations of claim 22. Therefore, claim 28 is rejected for the same reasons as claim 22.

42. As per claim 29:

Claim 29 essentially recites the same limitations of claim 23. Therefore, claim 29 is rejected for the same reasons as claim 23.

43. As per claim 30:

Claim 30 essentially recites the same limitations of claim 24. Therefore, claim 30 is rejected for the same reasons as claim 24.

44. As per claim 31:

Park, So, and Gorishek disclosed the system of claim 28, wherein the subsequent instruction is the first permanent instruction, wherein the first permanent instruction indicates a plurality of instructions from the second instruction set is to follow and permanently switches the decode logic from the first mode to the second mode (Gorishek: Figure 8 element 140, column 15 lines 46-67 continued to column 16 lines 1-3)(The Go instruction tells that there will be a large sequence of emulation processing to

come and that the mode of execution will change so that the emulation program is executed until a stop instruction occurs. Thus having the same functionality.).

45. As per claim 32:

Park, So, and Gorishek disclosed the system of claim 27, wherein the second permanent instruction indicates a plurality of instructions from the first instruction set is to follow and permanently switches the decode logic from the second mode to the first mode (Gorishek: Figure 8 element 140, column 15 lines 46-67 continued to column 16 lines 1-3)(The Stop instruction tells that the large sequence of emulation instructions has ended and that host processor instructions can continue to execute. Thus having the same functionality.).

46. As per claim 33:

The system of claim 27, wherein the system comprises a cellular telephone (Official notice is taken that the processing system could be part of a cellular telephone.).

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ohsuga et al. (U.S. 6,434,690), taught a microprocessor having a DSP and a CPU with a predecoder to determine type of instruction it is and sent it to the correct execution unit.

Worrell (U.S. 6,012,138), taught a variable length pipeline to execute two separate ISA's and executes in multiple modes that determine if the current instructions are native or emulated instruction from a non-native ISA translated to execute on the processor.

Dua et al. (U.S. 6,678,817), taught processing two ISA's by running emulated instructions that are fetched through fetch requests by the emulation engine.

Borrill (U.S. 6,496,922), taught supporting two ISA's by using on-the-fly hardware instruction translation by having multiple modes of execution.

Gorishek, IV et al. (U.S. 6,480,952), taught a host and coprocessor to execute native and foreign code.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
Art Unit 2183

RICHARD L. ELLIS
PRIMARY EXAMINER